

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants : Minchang Liang et al.
Application No. : Not yet available
Confirmation No. : Not yet available
Filed : Concurrently herewith
For : BIPOLAR TRANSISTORS WITH LOW BASE
RESISTANCE FOR CMOS INTEGRATED CIRCUITS
Group Art Unit :
Examiner :

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450


INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to 37 C.F.R. §§ 1.56, 1.97, and 1.98,
applicants hereby bring the attention of the Examiner to the
documents listed on the attached Form PTO-1449 (submitted in
duplicate).

A copy of each listed document is enclosed herewith.

Respectfully submitted,


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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)		Application Number	
		Filing Date	Herewith
		First Named Inventor	Minchang Liang
		Art Unit	
		Examiner Name	
Sheet	1	of	1
		Attorney Docket Number	A1385

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		A. HOKAZONO et al. "Source/Drain Engineering for Sub-100 nm CMOS Using Selective Epitaxial Growth Technique" (c) 2000 IEEE	
		A. SAMOILOV et al. "Properties and Applications of Strained Si/SiGe", Applied Materials Inc., April 17, 2002	
		J. ZHANG. et al. "n-Si/n-p-i SiGe/n-Si structure for SiGe microwave power heterojunction bipolar transistor grown by ultra-high-vacuum chemical molecular epitaxy" Journal of Applied Physics, Vol 86, No. 3, pp. 1463-1466, 1 August 1999 (c) American Institute of Physics	
		M. KUMAR, "A 3-D BiCMOS Technology Using Selective Epitaxial Growth (SEG) and Lateral Solid Phase Epitaxy (LSPE)", (c) 2001 IEEE	
		J.-M. HARTMANN, "Reduced Pressure - Chemical Vapor Deposition of Si/SiGeC heterostructures for future applications", CEA/LETI Annual Review 2002	
		R. CHAU, "Advanced Depleted-Substrate Transistors: Single-Gate, Double-Gate and Tri-Gate", 2002 International Conference on Solid State Devices and Materials (SSDM 2002), Nagoya, Japan 17/02	
		Z. KRIVOKAPIC, "High Performance 25 nm FDSOI Devices with Extremely Thin Silicon Channel" AMD, Technology Research Group (6/2003)	

Examiner Signature		Date Considered	
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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